REMARKS

The Office Action dated June 13, 2006 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto. Claims 1-6, 8-16, and 18-19 are pending and submitted for consideration.

Claims 1-7, 10, 11, and 14-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by *Huang* (U.S. Patent No. 6,728,910 B1 – hereinafter referred to as *Huang '910*). The Office Action took the position that *Huang '910* teaches each and every element recited in the rejected claims. Applicant traverses the rejection and respectfully submits that each of claims 1-7, 10, 11, and 14-17 recite subject matter that is not taught or disclosed by *Huang '910.*

Claim 1, the independent claim from which claims 2-9 depend, recites a method that includes determining if a memory is functional based on memory BIST data, selecting a redundant memory section if a portion of the memory is determined to be nonfunctional, determining if at least the selected redundant memory is functional according to a BIST, and updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant.

Claim 10 recites a system including means for determining if a memory is functional based on memory BIST data, means for selecting a redundant memory section if a portion of the memory is determined to be nonfunctional, means for determining if at

least the selected redundant memory is functional according to a BIST, and means for updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant.

Claim 11, the independent claim from which claims 12-19 depend, recites a system having a BIST capable of determining if a memory is functional, and self-adaptive logic, communicatively coupled to the BIST, capable of selecting a redundant memory section if a portion of the memory is determined to be nonfunctional, wherein the BIST is further capable of determining if at least the selected redundant memory is functional, and updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant.

Applicant submits that each of claims 1, 10, and 11 recite subject matter that is not taught or disclosed by *Huang '910*.

Huang '910 teaches a method for self-test and self-repair of a semiconductor memory device. A single built-in self-test (BIST) engine with an extended address range is used to test the entirety of memory, *i.e.*, both redundant and accessible memory portions, as a single array, preferably using a checkerboard bit pattern. In a first stage, faulty rows in each memory portion are identified and their addresses recorded. Known-bad rows in accessible memory are then replaced by known-good redundant rows, and the resulting repaired memory is retested in a second stage. During a second stage, repair of the accessible memory portion is verified, while defects among the redundant portion are ignored.

However, *Huang '910* does not teach or disclose determining if at least the selected redundant memory is functional according to a BIST and updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as recited in each of Applicant's independent claims 1, 10, and 11. The Office Action cites to column 9, lines 6-13 and column 3, lines 53-58 of *Huang '910* as teaching these features, however, careful review of the cited sections of *Huang '910* does not support this conclusion. More particularly, lines 6-13 of column 9 of *Huang '910* teach that when the BIST goes through the retesting process, it retests a combination of accessible and redundant rows that tested good in the first stage. There is no express teaching or disclosure of testing the "selected redundant memory" locations recited in Applicant's claims 1, 10, and 11. Further, there is no teaching or disclosure of updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as also recited in Applicant's independent claims 1, 10, and 11. Lines 53-58 of column 3 of *Huang '910* discuss the repair table and the substitution of the good (redundant) row into the second stage of the BIST test. There is no teaching or disclosure of updating a memory data structure to indicate that the selected redundant memory location that is being used to replace the non-functional memory location is updated in a redundant memory data structure as no longer being available as redundant memory data. Therefore, Applicant submits that *Huang '910* fails to teach or disclose each and every element recited in Applicant's independent clams 1, 10, and 11.

As such, reconsideration and withdrawal of the rejection of claims 1, 10, and 11, along with each claim depending therefrom, is respectfully requested.

Claim 12 stands rejected under 35 U.S.C. §103(a) as being obvious over *Huang '910* in view of *Huang '066* (U.S. Publication No. 20020136066A1 – hereinafter referred to as *Huang '066*). The Office Action took the position that *Huang '910* teaches each and every element recited in claim 12, except for the self adaptive logic limitations. However, the Office Action cites to *Huang '066* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicant's claimed invention. Applicant traverses the rejection and respectfully submits that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claim 12.

Huang '910 is discussed above. *Huang '066* teaches a system and method for a self-repairing memory that can be integrated with any BIST mechanism, without extensive modification to either the BIST or BISR mechanisms. A BISR "Wrapper" system interfaces the BIST engine to the BISR repair circuitry. The BISR Wrapper makes use of standard status signals present in any BIST engine, and directs the operation of the BISR circuitry. With the Wrapper, BISR operation need no longer be closely coupled to the operation or internal structure of the BIST. Consequently, modification of the BIST mechanism, *e.g.*, to improve fault coverage, can be implemented without influencing the BISR.

However, *Huang '066* does not teach, show, or suggest a BIST that is capable of updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as recited in claim 11, the independent claim from which claim 12 depends. As such, Applicant submits that *Huang '066* does not further the teaching of *Huang '910* to the level necessary to properly support an obviousness rejection. Therefore, reconsideration and withdrawal of the rejection of claim 12 is respectfully requested.

Claim 13 stands rejected under 35 U.S.C. §103(a) as being obvious over *Huang* in view of *Tanizaki* (U.S. Patent No. 6,993,696). Applicant notes that the Office Action did not indicate which *Huang* reference is referred to in this rejection, *i.e.*, *Huang '910* or *Huang '066*, and as a result thereof, Applicant presumes that the Office Action is citing to *Huang '910* in the rejection. The Office Action took the position that the *Huang* references teach each and every element recited in claim 13, except for the state of a pin. However, the Office Action cites to *Tanizaki* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicant's claimed invention. Applicant traverses the rejection and respectfully submits that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claim 13.

Both of the *Huang* references are discussed above. *Tanizaki* teaches a semiconductor memory device with a built-in self test circuit includes a semiconductor substrate, a memory cell array formed on the semiconductor substrate, an input buffer provided on the semiconductor substrate to receive externally applied data, a test circuit coupled to the memory cell array and the input buffer on the semiconductor substrate to store a program received through the input buffer to generate test data of the memory cell array according to the stored program to carry out testing of the memory cell array, and a select circuit selectively applying to the memory cell array test data applied from the test circuit and data applied from the input buffer depending upon a test operation and a normal operation.

However, *Tanizaki* does not teach, show, or suggest a BIST that is capable of updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as recited in claim 11, the independent claim from which claim 13 depends. As such, Applicant submits that *Tanizaki* does not further the teaching of the *Huang* references to the level necessary to properly support an obviousness rejection. Therefore, reconsideration and withdrawal of the rejection of claim 13 is respectfully requested.

Claims 8 and 18 stand rejected under 35 U.S.C. §103(a) as being obvious over *Huang* in view of *Aipperspach* (U.S .Patent No. 6,181,614). Again, the Office Action has not indicated which *Huang* reference is referred to in the rejection, and therefore, Applicant must address the rejection as if the Office Action intended to cite both *Huang*

references. The Office Action took the position that *Huang* teaches each and every element recited in claims 8 and 18, except for where the method of performed during the manufacturing process. However, the Office Action cites to *Aipperspach* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicant's claimed invention. Applicant traverses the rejection and respectfully submits that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claims 8 and 18.

The *Huang* references are discussed above. *Aipperspach* teaches a circuit arrangement and method of dynamically repairing a redundant memory array utilize dynamically-determined repair information, generated from a memory test performed on the redundant memory array, along with persistently-stored repair information to repair the redundant memory array. In one implementation, the persistent repair information is generated during manufacture to repair manufacturing defects in the array, with the dynamic repair information generated during a power-on reset of the array to address any additional faults arising after initial manufacture and repair of the array. Furthermore, repair of dynamically-determined errors may utilize otherwise unused redundant memory cells in a redundant memory array, thus minimizing the additional circuitry required to implement dynamic repair functionality with an array.

However, *Aipperspach* does not teach, show, or suggest a BIST that is capable of updating the redundant memory data structure to indicate that the selected redundant

memory section is no longer redundant, as recited in claims 1 and 11, the independent claims from which claims 8 and 18 depend. As such, Applicant submits that *Aipperspach* does not further the teaching of the *Huang* references to the level necessary to properly support an obviousness rejection. Therefore, reconsideration and withdrawal of the rejection of claims 8 and 18 is respectfully requested.

Claims 9 and 19 stand rejected under 35 U.S.C. §103(a) as being obvious over *Huang* in view of *Cheston* (U.S. Publication No. 20030014619A1). Again, Applicant notes that the Office Action did not indicate which *Huang* reference is referred to in this rejection, *i.e.*, *Huang '910* or *Huang '066*, and as a result thereof, Applicant presumes that the Office Action is citing to *Huang '910* in the rejection. The Office Action took the position that *Huang* teaches each and every element recited in claims 8 and 18, except for where the method is performed during circuit power up. However, the Office Action cites to *Cheston* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicant's claimed invention. Applicant traverses the rejection and respectfully submits that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claims 9 and 19.

The *Huang* references are discussed above. *Cheston* teaches a method and system for recovering a master boot record within a data processing system. In the method, a master boot record recovery setup utility is invoked by a user. In response to invoking

the master boot record recovery utility, the master boot record in a first bootable device is copied to an alternate non-volatile storage device. A recovery flag is set within BIOS indicating that the MBR has been securely copied. In response to a failed boot attempted from the first boot device, the copy of said master boot record within said alternate non-volatile storage device is accessed and utilized to boot the system.

However, *Cheston* does not teach, show, or suggest a BIST that is capable of updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as recited in claims 1 and 11, the independent claims from which claims 9 and 19 depend. As such, Applicant submits that *Cheston* does not further the teaching of the *Huang* references to the level necessary to properly support an obviousness rejection. Therefore, reconsideration and withdrawal of the rejection of claims 8 and 18 is respectfully requested.

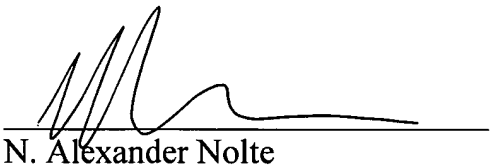
In conclusion, Applicant submits that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest a BIST that is capable of updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as recited in each of Applicant's independent claims. As such, reconsideration and withdrawal of the rejection of the claims is respectfully requested. Claims 1-6, 8-16, and 18-19 are pending and submitted for consideration.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by

telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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